Delayed Switching in Memristors and Memristive Systems

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***Abstract*—It was found that the switching in a memristor takes place with a time delay (this peculiar feature is named "the delayed switching"). This feature has been verified by a circuit-based experiment. The physical interpretation of this phenomenon is that an electron element possesses certain inertia, i.e., charge q or flux φ is inertial with the tendency to remain unchanged (settle to some equilibrium state). It cannot respond as rapidly as the fast variation in the excitation waveform and always takes a finite but small time interval to change its resistance value, as it must take place in a memristor or memristive system. In addition, a potential application of using this feature in ultradense computer memory has been discussed.**

***Index Terms*—Electronic device, memristive system, memristor, random access memory, resistively switching.**

I. Introduction

THE MEMRISTOR was formulated and named by Leon Chua in 1971 [1]. Chua strongly believed that a fourth device existed to provide conceptual symmetry with the resistor, inductor, and capacitor. Chua also used memristors to model an amorphous "Ovonic" threshold switch and an electrolytic E-cell, to process many types of signals, and to generate various waveforms such as the staircase waveform [1].

Williams announced the discovery of a memristor based on a nanoscale thin film of titanium dioxide in 2008 [2]. In addition, there were the following claims to have developed other types of memristors: 1) spin memristive systems [3]; 2) polymeric memristors [4]; and 3) manganite memristive systems [5]. These claimed memristors broaden the possible range of memristors.

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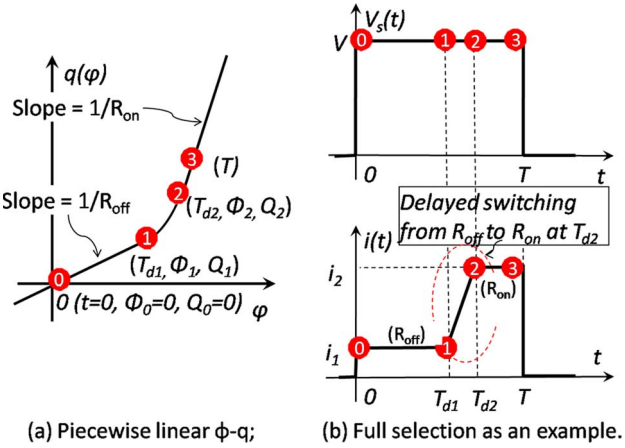

Fig. 1. (a) Approximation of Chua's piecewise linear model [1], in which it takes a finite but small time interval for a memristor to switch completely from a high resistance to a low resistance or vice versa. (b) Memristor's delayed-switching property: The switching from one resistance state to another due to an input voltage pulse takes place with a time delay $T_d \approx T_{d1} \approx T_{d2}$. T_d increases as the amplitude V of the square-wave voltage pulse $Vs(t)$ decreases. The numbers 0–3 label the successive time points during a square-wave period T.

II. Delayed-Switching Property of Memristors

It was found that the switching in a memristor takes place with a time delay (this peculiar feature is named "the delayed switching"). Conceptually, a memristor element links charge q and flux φ, and the charge is a single-valued function of the flux [1], [6], [7]. Fig. 1(a) approximates Chua's piecewise linear model [1], in which a transition (from T_{d1} to T_{d2}) divides the curve into two linear pieces: OFF-resistance $(R_{\rm off})$ and ON-resistance $(R_{\rm on})$. It is assumed that $\varphi_0 = 0$ and $q_0 = 0$ at $t = 0$.

In a delayed-switching test, a voltage $V_s(t)$ is applied to the memristor and a current $i(t)$ is imposed. $R(q) = d\varphi/dq$ has the unit of resistance, and in the case where the $\varphi - q$ curve is approximately a piecewise straight line, we obtain $R(q) = R_{\rm off}$ or $R_{\rm on}$ that is a constant. In other words, a memristor behaves like an ordinary resistor at a given instant of time t'; its resistance depends on the complete history of the current, i.e., the time integral of the current from $t = -\infty$ to $t = t'$. Therefore, the state equation of a memristor can be given by

$$q(t) = \int i(t)dt = \int \frac{V \cdot dt}{R} = \frac{V}{R} \cdot t. \qquad (1)$$

At the transition where $t = T_{d1,2}$, we have $q(T_{d1,2}) = Q_{1,2}$ and $\varphi(T_{d1,2}) = \Phi_{1,2}$. Therefore

$$Q_{1,2} = \frac{V}{\frac{\phi_{1,2}}{Q_{1,2}}} \cdot T_{d1,2} \tag{2}$$

$$T_{d1,2} = \frac{\phi_{1,2}}{V}, \qquad \text{i.e., } T_{d1} = \frac{\phi_1}{V} \quad T_{d2} = \frac{\phi_2}{V}. \tag{3}$$

An examination of (3) shows that, for a given φ–q curve [Fig. 1(a)], the time delay T_d ($\approx T_{d1} \approx T_{d2}$) decreases as the amplitude V of the square-wave pulse in Fig. 1(b) increases. Hence, corresponding to the square-wave pulse $V_s(t)$ with amplitude V, we obtain the waveforms for the output current $i(t)$, as shown in Fig. 1(b). The switching from the high resistance (R_{off}) to the low resistance (R_{on}) takes place with a time delay T_d ($\approx T_{d1} \approx T_{d2}$) after the application of an input square-wave voltage [Fig. 1(b)]. If the input voltage is removed before the switching takes place, i.e., the width T of the input voltage pulse is smaller than $T_d \approx T_{d1} \approx T_{d2}$, the memristor remains unaltered. Therefore, in order to switch a memristor, T should be chosen in such a way that $T_d < T$.

This property results from the (approximately) piecewise linear nature of the φ–q curve in Fig. 1(a). A full selection operation in Fig. 1(b) means a full voltage V is applied across the memristor. A half selection operation (not shown in Fig. 1) means only a half voltage $V/2$ is applied.

The current amplitudes through the memristor are given by

$$i_1 = \frac{V}{R_{\text{off}}} \tag{4}$$

$$i_2 = \frac{V}{R_{\text{on}}} \tag{5}$$

where R_{off} and R_{on} represent the resistances corresponding to the two linear pieces of the memristor φ–q curve and where $(Q_{1,2}, \Phi_{1,2})$ is the coordinate of the transition between these two pieces (at $t = T_{d1,2}$).

The approximately piecewise linear nature manifests itself vividly in the form of a delayed-switching property, where the switching versus a square-wave input takes place with a time delay. In other words, it is a natural consequence of the approximately piecewise linear φ–q curve in a memristor. The physical interpretation of this phenomenon is that a memristor possesses certain inertia, i.e., charge q or flux φ is inertial with the tendency to remain unchanged (settle to some equilibrium state). It cannot respond as rapidly as the fast variation in the excitation waveform and always takes a finite but small time interval for the memristor to change its resistance value. In other words, there is a delay between the application of the voltage and the change in the memristance value. This fact is natural if the state variable that determines the memristance is not as "mobile" as the excitation. In principle, this delayed waveform should be reproduced by any generic "dopant-drift" model such as HP's titanium dioxide memristor [2].

The memristor was generalized to memristive systems [6]. The delayed-switching feature should be extended to memristive systems in the sense that it is a general observation that the state variable is not as "mobile" as the excitation.

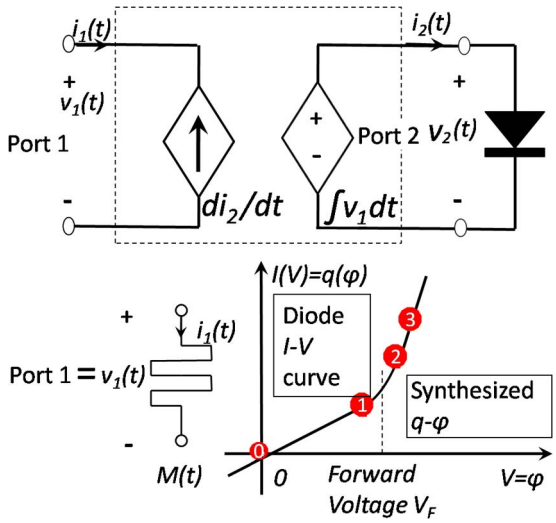

Fig. 2. Circuit realization of a memristor using controlled active sources and a diode (a nonlinear element). The circuit is equivalent to a memristor with the shown φ–q curve that is transformed from the diode's V–I curve.

A pure memristor is a particular case of memristive systems, namely, when the memristance $R(q)$ depends only on charge q. Nevertheless, a memristive system has a set of state variables, which would make (1)–(5) more complex.

III. Circuit-Model Experiments of Delayed Switching

As mentioned in Section I, a number of exemplified memristors (titanium dioxide memristor, spin memristor, polymeric memristor, manganite memristor, etc.) broaden the possible range of memristors. In 2009, Ventra et al. extended the notion of memristive systems to capacitive and inductive elements [8]. Since there exists a controversy as to the memristance behavior of these specific devices [9], we used Chua's "circuit model" [1], [6] to construct a memristor. Then, we measured its delayed-switching property and the behavior in full selection and half selection, respectively. The advantages of physically constructing and characterizing a circuit model of a memristor include a broad generalization of memristors to an interesting class rather than a specific element and the ease of changing the parameters.

According to Chua's circuit model theory, a memristor with any prescribed φ–q curve can be realized by using an active circuit in connection with an appropriate nonlinear element [1], [6]. In Fig. 2, the V–I curve of a diode (a nonlinear element) connected in Port 2 (v_2, i_2) is transformed into the φ–q curve of a synthesized memristor in Port 1 (v_1, i_1).

To demonstrate the delayed-switching property possessed by the synthesized memristor, a oscilloscope is used to trace the voltage $v(t)$ and current $i(t)$ of the memristor. The Zener diode BZX79C permits a forward voltage of 0.8 V. The waveforms $v(t)$ and $i(t)$ in Fig. 3(a) (half selection with an input voltage of 10 mV) and Fig. 3(b) (full selection with an input voltage of 20 mV) are measured with a 10-kHz square-wave input signal. A delayed switching (around 0.4 ms) is clearly seen in Fig. 3(b). The corresponding V–I loops are also measured in the figure.

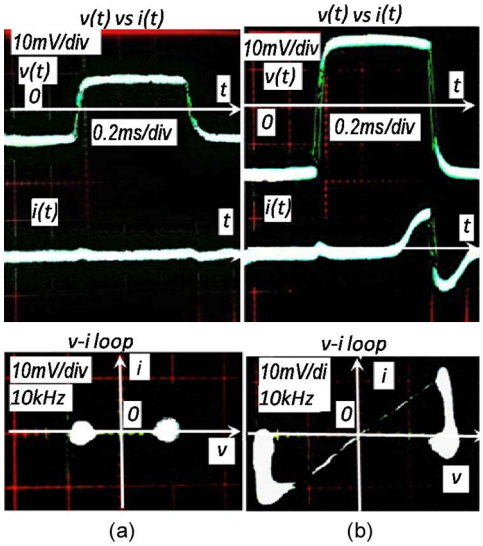

Fig. 3. Measured $v(t)-i(t)$ waveforms and $v-i$ loops for (a) half selection and (b) full selection. A delayed switching is clearly seen in full selection. The $v-i$ loop always passes through the origin. As the voltage amplitude decreases, the $v-i$ loop degenerates into a pure resistor with a single resistance value (no switching).

A comparison between these experimental waveforms in Fig. 3 and those for Chua's piecewise linear model [1] in Fig. 1 reveals a striking resemblance. The synthesized memristor in Fig. 2 seems to simulate not only the exact shape of the stepwise waveforms but also the attendant decrease of the time delay T_d with increasing amplitude V.

As predicted by Chua [1], [6], one fingerprint of a memristor is its zero-crossing property. Observe that, in spite of the memory effect which normally introduces phase shifts in conventional memory systems (e.g., a capacitor memory), the output of a memristor is zero whenever the input is zero, and hence, the input–output $v-i$ loop always passes through the origin, as shown in the bottom of Fig. 3. The $v-i$ loops reflect the delayed-switching behavior of the memristor: It begins with a high resistance, and as the voltage increases, the current slowly increases. When the breakpoint is overtaken, the resistance drops, and the current increases more rapidly with increasing voltage until the maximum is reached. Then, when the voltage decreases, the current decreases but more slowly. When the voltage turns negative, the resistance of the device increases, resulting in a symmetric switching loop.

The amplitude/frequency response of a memristor is particularly interesting to a practical memory application. As shown in the bottom of Fig. 3, as the excitation amplitude decreases or, equivalently, the excitation frequency increases toward $T < Td$, the Lissajous V–I loop shrinks and turns into a straight line passing through the origin. This implies that the hysteretic effect of a memristor decreases as the voltage amplitude decreases (equivalently, the frequency increases), and hence, it eventually degenerates into a pure resistor with a single resistance value (no switching).

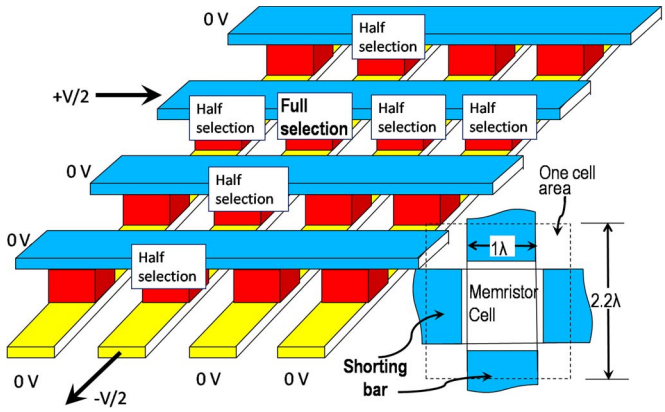

Fig. 4. Transistor-free crossbar architecture. "Full selection" means a full voltage V is applied across the two wires with the desired memristor at the intersection. "Half selection" means only a half voltage $V/2$ is applied across the (undesired) memristor. An inset shows low-resistance shorting bars running between cells. λ is the resolution limit of the lithography used to fabricate the memory cells. The minimum linewidth is λ, and the minimum distance between lines is 1.2 λ; thus, one cell area is 4.84 λ^2 [10].

IV. Transistor-Free MR-RAM

The peculiar property of delayed switching inspires us to apply it to a transistor-free crossbar architecture [10] for memristor-based random access memory (MR-RAM) (Fig. 4). When $\pm V/2$ are applied to a word line and a bit line, respectively, the combined voltages drop V at the intersection of the energized word and bit lines will switch the resistance state of the memristor located at the intersection (full selection). "Half selection" occurs when a memristor cell is selected by only one word line or bit line. Obviously, those half-selected memristors should not be written (altered). An analytical model [10] shows that memristors can be packed at least twice as densely as semiconductors, due to the absence of a transistor, achieving a significant breakthrough in storage density.

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